

Design of Large Built-in Self-Test Programmable Logic Arrays

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ABSTRACT

This paper presents a way to optimize design of large built-in self-test (BIST) programmable logic arrays (PLAs). These PLAs can be tested at clock speed with function independent test set. Hardware overhead of the design is low compared to other techniques. In the design, test pattern generators are simple shift registers connected in ring counter form. Response evaluator circuit is a signature analyzer. A two bit binary counter and two D flip-flops automate the design process and reduce the number of test control pins. The PLA can detect all stuck-at, crosspoint, bridging as well as stuck-open faults.

ABSTRAK

Kertas ini membentangkan suatu kaedah untuk mengoptimum reka bentuk tatasusun logik uji-diri bina-dalam boleh program yang besar. Tatasusun berkenaan boleh diuji pada kelajuan jam dengan set ujian yang tidak bersandar kepada fungsi. Overhed perkakasan reka bentuk tersebut adalah rendah berbanding dengan kaedah-kaedah lain. Dalam reka bentuk ini, penjana corak ujian adalah pendaftar-pendaftar anjakan mudah yang disambung dalam bentuk pembilang gelang. Litar penilai respons adalah sebuah penganalisis tanda tangan. Suatu pembilang perduaan dua bit dan dua flip-flop jenis D mengautomasi proses reka bentuk dan mengurangkan bilangan pin-pin kawalan ujian. Tatasusun berkenaan boleh mengesan semua kegagalan lekat-pada, titik lintas, penitiran dan juga kegagalan lekat-buka.

INTRODUCTION

Regular structure and computer aided synthesis techniques have made the programmable logic array (PLA) an important tool for implementing combinational logic circuits as well as state machines. Commercial microprocessors like Intel's 80386, Motorola's 68020 and AT&T's WE32000 contain several PLAs in their designs.

PLAs, which are conceptually AND-OR planes, are difficult to test by random testing and conventional test techniques due to their large fan-in requirements. Recent approach is to incorporate on-chip built-in self-test (BIST) techniques to make PLAs testable. A practical BIST PLA should meet the following requirements: (1) increased fault coverage, (2) ease of test application, (3) reduced testing time, (4) at speed testing capability, (5) simple test pattern generator, and (6) simple and reliable response evaluator with low hardware overhead (Upadhyaya & Saluja 1988; Reddy & Ha 1987). A

number of BIST PLA designs have been proposed in literatures (Upadhyaya & Saluja 1988; Fujiwara 1988; Saluja *et al.* 1983). These techniques differ in test application approach, BIST hardware organization and response evaluation techniques. PLA testing can be of three types, (1) random testing (Fujiwara 1988) (2) function dependent testing (Reddy & Ha 1987) and (3) function independent testing or universal testing (Upadhyaya & Saluja 1988; Saluja, *et al.* 1982; Fujiwara & Kinoshita 1981; Liu & McCluskey 1988). Random testing is crippled with high testing time. Function dependent testing is rather complex. Testing using universal test set is attractive for its simplicity and reduced testing time. Response evaluators can be (1) multiple input shift register (MISR) signature analyzer (Saluja *et al.* 1983, Daehn & Mucha 1981), (2) parity checker (Fujiwara & Kinoshita 1981; Fujiwara 1984; Liu & McCluskey 1983) and (3) binary counter (Upadhyaya & Saluja 1988). Each of these techniques has its unique fault detection capability.

Common industry practice is to test PLAs pseudorandomly using linear feedback shift register (LFSR) as test pattern generator. It usually limits the largest size of a BIST PLA to 20 inputs. Fujiwara (1988) proposed a design technique of PLAs with random pattern testability. He segmented bit lines into small groups and used a decoder to select any one group at a time for random testing. He used a probabilistic approach on the fault coverage estimation of stuck-type and cross-type faults. Although his technique is an improvement to random pattern testable PLAs, it requires a number of test control pins and its testing time can be considerably high for large PLAs.

Daehn and Mucha (1981) used a deterministic test set (also known as universal test set) and three built-in logic block observer (BILBO) registers attached to bit lines, product lines and output lines as response evaluators. Area overhead of such a design is quite high.

Fujiwara and Kinoshita (1981) proposed another BIST PLA design technique with universal test set. They used parity property in response evaluation. They proceeded by selecting one bit line and one product line at a time and checked the parity. But cascaded exclusive OR (XOR) gates occupy large area. These cascades have a long delay which compels to test PLAs at a slower test clock speed. Liu and McCluskey (1988) extended Fujiwara and Kinoshita's (1988) ideas and used sequential parity checking technique in response evaluation. They used parity checking register at the output lines which functions as a parity counter and a shift register (Liu & McCluskey 1988). This design can be tested at system clock speed. They used dynamic circuitry in the design of test pattern generator (TPG) cells, product line selector, and parity checking register cells. Although this technique offers high fault coverage with reduced hardware overhead, it cannot detect even number of faults in a row because of its parity adding property. To overcome this problem, they set a design rule that no two adjacent output lines be connected to an even number of common product lines. But such a design rule is not attractive to designers. For a large number of output lines, the size of the parity checking register can become quite high.

Upadhyaya and Saluja (1988) used a counter as response evaluator. This design can be tested at clock speed and its fault coverage is quite high. The counter counts crosspoint devices of each column and compares it with the reference value. The reference value is stored in a second counter. It implies

a stringent rule of arranging product lines of PLAs with ascending number of crosspoints (only an increment of one is allowed). In the case of missing number in the ascending sequence, extra product line or lines should be inserted with the missing number of crosspoint devices. For repeated number of crosspoint devices, an extra output line should be added in the OR plane to control increment of reference counter. Such design constraint may incur unpredictable amount of hardware overhead. Their design constraints are not always convenient to commercial PLA designers.

In this paper, a method to optimize BIST PLA design for universal tests is presented. The design approach uses a two input signature analyzer as response evaluator. It has no hard and fast design constraint. The design is suitable for commercial BIST PLA design. Its fault coverage is very high and comparable to other designs (Upadhyaya & Saluja 1988; Liu & McCluskey 1988). It can detect stuck-at, stuck-open, crosspoint and bridging faults.

The rest of the paper is arranged in the following way: section II describes the design approach and test scheme, section III gives the test set and analyzes fault detection capability of the PLA, section IV makes a general discussion and section V ends the paper with concluding remarks.

DESIGN APPROACH

The design of the proposed PLA makes use of the fact that MOS PLAs are implemented as two stage NOR-NOR gates, although they are conceptually two stage AND-OR gates. It uses test pattern generators which can generate walking one and walking zero test patterns. A two input signature analyzer is used as a response evaluator. Test responses are collected for signature analysis through two extra lines incorporated in the PLA. One line is inserted in the OR plane parallel to the output lines having crosspoint devices with all the product lines and another line is inserted parallel to the product lines having crosspoint devices with all the output lines.

DEFINITIONS

The PLA is assumed to have l inputs, m product lines and n output lines. Input lines are denoted as $\{I_i\}$, bit lines as $\{B_i\}$, product lines as $\{P_i\}$ and output lines as $\{O_k\}$. The array consists of $(2l + n)$ rows and m columns. The PLA is denoted as (l, m, n) PLA.

Definition 1 A crosspoint is the intersection of a row with a column. An FET device may or may not exist at a crosspoint.

Definition 2 A crosspoint device is the existence of an FET at a crosspoint. A missing (extra) crosspoint device is an unintended absence (presence) of an FET at a crosspoint.

Definition 3 A stuck-open fault is an open circuit defect in the gate or drain or source interconnections of a transistor or strongly shifted voltages. Its effect is like a memory type device. Certain input patterns do not alter the output state either to low or to high. Instead, load capacitance retains the previous state at the output (Johnson 1989; Fritzmeir et al. 1989).

Definition 4 Walking one (zero) test pattern is a test set where all the bits in the pattern are zero (one) except one (Daehn & Mucha 1981). This one (zero) is shifted serially along the shift register (Table 1).

TABLE 1. Universal test set

Walking one test vector	Walking zero test vector
0000...00	1111...11
1000...00	0111...11
0100...00	1011...11
0010...00	1101...11
...	...
...	...
0000...10	1111...01
0000...01	1111...10

ORGANIZATION OF THE BIST PLA

The BIST PLA is organized in such a way that the test set can verify existence of crosspoint devices at each crossing of a row with a column. This is done by sensitizing a row and a column at a time. Test responses are collected at the signature analyzer input. The block diagram of the BIST PLA is shown in Figure 1. It contains the following functional blocks:

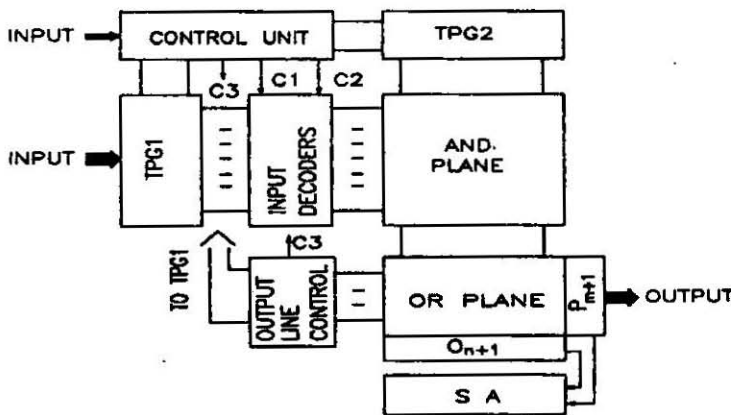


FIGURE 1. Block diagram of the proposed BIST PLA

1. Input Decoders A 2-input NOR gate is inserted on each bit line. The second input of the NOR gates on noncomplemented bit lines are tied together. It functions as a control input and is labeled as C1. Similarly, a second control input is constructed for the complemented bit lines and it is labeled as C2. A logic high on the control input places the corresponding bit lines to zero. C1 and C2 are active low. Say, even numbers refer to non-complemented bit lines and odd numbers refer to complemented bit lines.

2. OR Plane Row Selector These buffers sensitize rows in the OR plane. A control input C3 is used to switch between normal mode and test mode. They are shown in Figure 1 as output line control block.

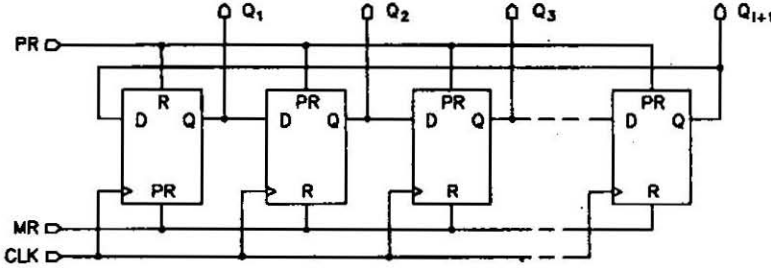


FIGURE 2. Test pattern generator. Ring counter structure

3. Row Test Pattern Generator (TPG1) It is an $(l + 1)$ bit shift register arranged in the form of a ring counter (Figure 2). The output of the last cell is fed back to the input of the first cell. At the beginning of test, the first cell is preset to 1 and other cells are reset to zero. One extra bit in the register is added to set all the bit lines to zero. TPG1 can generate walking zero test pattern by resetting one of the cells to zero and presetting others to one. Walking zero test pattern can also be obtained from the inverted outputs of the flip-flops of TPG1 while it is generating walking one test pattern.

4. Column Test Pattern Generator (TPG2) It is an $(m + 1)$ bit shift register arranged in the form of a ring counter. Its purpose is to generate walking zero test pattern to sensitize one column (i.e. product line) at a time.

5. Control Unit (CU) It consists of one 2-bit binary counter and two D flip-flops. They are used to automate test sequences by selecting noncomplemented bit lines, complemented bit lines and rows in the OR plane, respectively. Schematic of the control unit is shown in Figure 3.

6. Extra Row (O_{n+1}) An extra row (O_{n+1}) is inserted in the OR plane having crosspoint devices with each of the product lines. This row can sense responses of a row with a column in the AND plane. It realizes the function,

$$O_{n+1} = P_1 + P_2 + \dots + P_m$$

7. Extra Column (P_{m+1}) An extra column (P_{m+1}) is inserted in the OR plane having crosspoint devices with each of the output lines. Its purpose is to sense response of each crossing of a row with a column in the OR plane. Outputs of the extra row and the extra column are fed to the signature analyzer (SA) inputs as shown in Figure 1. The extra column realizes the function,

$$P_{m+1} = O_1 + O_2 + \dots + O_n$$

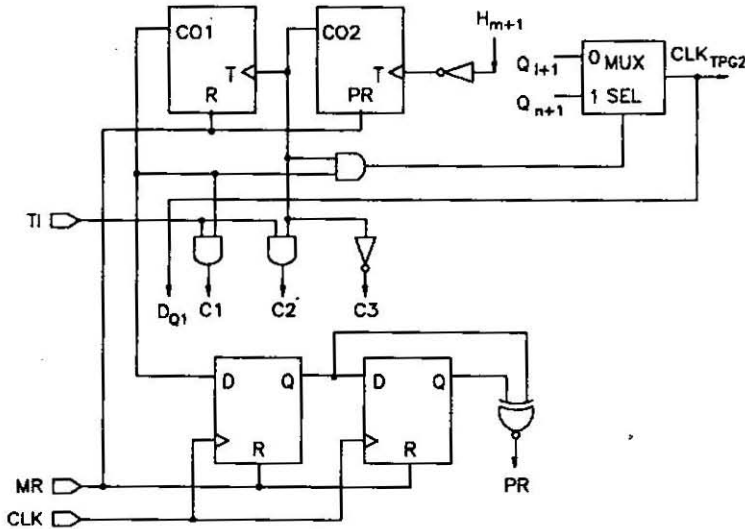


FIGURE 3. Schematic diagram of the control unit (CU)

8. Signature Analyzer (SA) A two input signature analyzer (SA) can be a linear feedback shift register (LFSR) or a cellular automata (CA) register. The length of the SA is of designer's choice.

PLA TEST

PLA test is initialized by resetting all the registers and flip-flops through the master reset (MR) input and setting test initialize (TI) input high. Outputs of the two bit binary counter in the control unit (CU) are labeled CO1 and CO2. CO1 is connected to the control input C1 and CO2 is connected to the control input C2 through two input AND gates Figure 3. Other inputs of the two input AND gate are tied to the TI line. At the beginning of the test, the counter is set as follows: CO1 = 0 and CO2 = 1. It selects noncomplemented bit lines for test, while the complemented bit lines and output lines are reset to zero. TPG1 generates walking one test pattern. It is referred to as STEP ONE.

STEP ONE In STEP ONE, test is performed on each crossing of noncomplemented bit lines with the product lines. The test procedure is shown in Table 2.

Zero is shifted in TPG2 by controlling its clocking sequence by the output of the $(l + 1)$ th cell of TPG1. One extra cell is added to TPG1 register to produce all zero test pattern. Similarly, the length of TPG2 is $(m + 1)$. This is to generate all one test pattern in TPG2.

The two-bit counter counts the end sequence of STEP ONE. This is done by connecting the inverted output of the $(m + 1)$ th cell of TPG2 to the toggle input (T2) of the counter.

STEP TWO At the end of STEP ONE, counter values will toggle. New reading of the counter is as follows: CO1 = 1 and CO2 = 0. It causes the following changes:

(1) noncomplemented bit lines are deselected and complemented bit lines are selected for test,

(2) two D flip-flops in the CU preset TPG1 to 0111...11 i.e., TPG1 is initialized to generate walking zero test pattern.

In STEP TWO each crossing of the complemented bit lines with the product lines is verified. At the end of STEP TWO, the CU counter toggles and assumes new value, CO1 = 1 and CO2 = 1.

STEP THREE With the new value in the CU counter, the following operations take place:

- (1) control inputs C1 and C2 deselect all the bit lines,
- (2) control input C3 selects rows in the OR plane for test.

TABLE 2. Test sequences

/*TEST NONCOMPLEMENTED BIT LINES IN THE AND PLANE */
STEP ONE:

```
{
  C1 = 0; C2 = 1; C3 = 1;
  FOR i = 1 TO m DO
    {
      SHIFT ZERO; /* TPG2 selects product line Pi */
      FOR j = 1 TO l DO
        SHIFT ONE; /* TPG1 selects noncomplemented bit lines B2j */
      }
    }
}
```

/* TEST COMPLEMENTED BIT LINES IN THE AND PLANE */
STEP TWO:

```
{
  C1 = 1; C2 = 0; C3 = 1;
  FOR i = 1 TO m DO
    {
      SHIFT ZERO; /* TPG2 selects product line Pi */
      FOR j = 1 TO l DO
        {
          SHIFT ZERO; /* TPG1 selects complemented bit lines B2j-1 */
        }
      }
    }
}
```

/* TEST OR PLANE */
STEP THREE :

```
{
  C1 = 1; C2 = 1; C3 = 0;
  FOR i = 1 TO m DO
    {
      SHIFT ZERO; /* TPG2 selects product line Pi */
      FOR j = 1 TO n DO
        {
          SHIFT ZERO; /* TPG1 selects rows in the OR plane Oj */
        }
      }
    }
}
```

If $n > l$, feedback in TPG1 should occur from the $(n + 1)$ th cell of the register during OR plane testing. Also, the clock input of TPG2 should be driven by the $(n + 1)$ th cell output of TPG1 ($n < l$ is assumed). A two input multiplexer (MUX) is placed in the CU. In STEP THREE, the MUX will change feedback point of the TPG1 and the clock input of TPG2 from $(l + 1)$ th to $(n + 1)$ th cell. If $n = l$, the MUX is not necessary. If $n > l$, the total length of TPG1 will be $(n + 1)$. Walking zero test pattern is required to select output lines in the OR plane. TPG1 keeps generating this test set.

PLA TEST SETS AND FAULT DETECTION

The proposed BIST PLA is designed for universal test sets. It uses a two input signature analyzer for test response evaluation. The PLA is capable of detecting the following faults: (1) all single and multiple crosspoint faults in the AND plane and in the OR plane, (2) bridging faults between bit lines, product lines as well as output lines, (3) all single and multiple stuck-at faults, (4) stuck-open faults in the pull-up devices. Walking one and walking zero test sets can be grouped into 5 sets as shown in Table 3. In Table 3, B, C, and H refer to bit lines, control lines and product lines respectively. They are explained in the subsequent discussions.

A: The test set A can detect (a) all single and multiple crosspoint faults in the AND plane and in the OR plane, (b) bridging faults between bit lines and between output lines and (c) all stuck-at faults.

Proof (1) Since test set A verifies each crossing of a row with a column (in both the AND and the OR planes), any missing or extra crosspoint device faults will cause erroneous sequence of responses in the signature analyzer input. Hence, all single and multiple crosspoint faults in the AND and the OR planes that generate erroneous sequence of responses will be detected.

(2) MOS bridging faults are modelled as logically ANDing (wired-AND) the affected lines. Since at any time, the test set A sensitizes only one bit line to one and others to zero, a bridging fault will pull the sensitized bit line down to zero. It will make all the devices controlled by the bit line as missing devices. This response is easily detected by the SA. Similar effects (wired-AND) are realized for bridging faults between product lines and between output lines. The signature analyzer can easily recognize such faults.

(3) Stuck-at zero faults have similar effect as missing crosspoint device. Stuck-at one faults also behave similarly as missing crosspoint device faults. Therefore, test set A can detect any (single or multiple) stuck-at faults on both the AND and the OR planes (Upadhyaya & Saluja 1988; Liu & McCluskey 1988).

B: Test sets B and C followed by test set A can detect stuck-open faults in the pull-up devices.

Proof Stuck-open faults in the pull-up devices can be detected by resetting the line to zero and then setting it to one (Liu & McCluskey 1987, 1988). Test set B resets the output line O_{n+1} and the product line P_{m+1} , and in the following step, test set A sets O_{n+1} and P_{m+1} lines to one at least once. Hence, stuck-open faults in the pull-up devices of the output line O_{n+1} and extra column P_{m+1} are detected.

TABLE 3

				Test Set A (1)										
B_2	B_4	B_{2i}	B_{2i}	C_1	C_2	C_3	H_1	H_2	H_i	H_m				
0	0	1	0	0	1	1	1	1	0	1				
				Test Set A(2)										
B_1	B_3	B_{2i-1}	B_{2i-1}	C_1	C_2	C_3	H_1	H_2	H_i	H_m				
0	0	1	0	1	0	1	1	1	0	1				
				Test Set A(3)										
O_1	O_2	O_i	O_n	C_1	C_2	C_3	H_1	H_2	H_i	H_m				
0	0	1	0	1	1	0	1	1	0	1				
											Test Set B			
B_1	B_2	B_i	B_{2i}	O_1	O_2	O_i	O_n	C_1	C_2	C_3	H_1	H_2	H_i	H_m
0	0	0	0	0	0	0	0	-	-	-	1	1	1	1
											Test Set C			
B_1	B_2	B_i	B_{2i}	O_1	O_2	O_i	O_n	C_1	C_2	C_3	H_1	H_2	H_i	H_m
0	0	0	0	0	0	0	0	-	-	-	0	0	0	0

The test set B resets each product line to zero and then the test set A sets it to one. It can detect stuck-open faults in the pull-up devices of the product lines. Similarly, the test set A also detects stuck-open fault in the pull-up devices of the output lines.

DISCUSSION

The proposed BIST PLA design technique is simpler compared to other techniques. Its faults coverage is comparable to other design techniques (Upadhyaya & Saluja 1988; Liu & McCluskey 1988). Its hardware overhead is also low. Its control unit (CU) has unique features of automating test scheme and reducing the number of test inputs. Following discussions will elaborate aspects of the present design.

1. Test Input Overhead If the master reset (MR) input is considered part of the system, test initialize (TI) input is the only test control pin overhead.

2. Area Overhead Area overhead elements in the PLA are two test pattern generators (TPG1 and TPG2), an additional row and an additional column, modified input decoders and response evaluators.

In TPG1, the number of register cells is $(l + 1)$ for $(l \leq n)$. This number is less than half the size used in Upadhyaya and Saluja (1988). Upadhyaya and Saluja (1988) used $(2l + n)$ cells. Liu and McCluskey (1988) used l -cell register and one extra product line with cross point devices with all the bit lines to realize NOR of all the states of the bit lines. Adding one extra cell is much more economic than adding one extra product line.

In TPG2, the number of register cells is $(m + 1)$, which is one more than that of Upadhyaya & Saluja (1988). Liu & McCluskey (1988) used a Johnson counter with a two level decoder. It requires much less hardware overhead than others. Such a TPG2 can also be used in the present design.

TABLE 4. Hardware overhead
(Units in the Table show number of FET devices)

	TPG1	TPG2	RE	Input Decoder	CU	Extra Columns & rows
A	$12l$	$5m+8$	$16n$	$8l$	-	$2l+m$
B	$9(2l+n)$	$9m$	$22L$	$8l$	-	$m+n$
C	$12(l+1)$ (if $l > n$) $12(n+1)$ (if $n > l$)	$9m+8$	$8X+6Y$	$8l$	84	$m+n$

$L = \lceil \log_2(l+n) \rceil$, 1 flip-flop = 8 FET, 1 XOR = 6 FET, X = Size of the signature analyzer (SA), Y = Number of XOR gates required for the SA. A = Design in Liu & McCluskey (1987), B = Design in Upadhyaya & Saluja (1988) and C = Proposed Design

TABLE 5. Hardware overhead (an example)
(Units in the Table show number of FET devices)

Example PLA $x2dn$ as listed in Upadhyay & Saluja (1988). $l = 82$, $m = 104$, $n = 56$

	TPG1	TPG2	RE	Input Decoder	CU	Extra Column & row	Total	Total (TPG2 in Liu & Mc Cluskey (1988))
A	984	528	896	656	-	268	3332	3332
B	1980	936	176	656	-	160	3908	3500
C	996	944	94*	656	84	160	2930	2518

* The signature analyzer is assumed to be an 8 bit LFSR.

TABLE 6. Test length

	No. of Test Pattern	Test Time per Pattern (ns)	Total Test Time (ns)
A	$2(m+1)(l+1)$	10	17.430×10^4
B	$m(2l+n)+m$	10	22.984×10^4
C	$(m+1)(2l+n+1)$	10	23.205×10^4

Overhead for modified input decoders can be compared to other design methods (Liu & McCluskey 1987; Upadhyaya & Saluja 1988). Additional control buffer is necessary for the row selection in the OR plane.

The control unit (CU) requires only four D flip-flops, one two input multiplexer and 5 gates. This overhead is negligible for large PLAs. Its added advantage is reduced number of test control inputs.

Parity-check register with each output line as response evaluator (RE) may become area intensive for PLAs with large number of output lines even though a dynamic design with reduced number of transistors is used. Overhead for counter RE can be small but it has a stringent constraint that ascending sequence of crosspoint device numbers on subsequent product lines should be maintained. It requires addition of extra product line (lines) where two neighbouring product lines do not have ascending number of crosspoint devices of difference one. A two input signature analyzer is a good solution to above problems, where designers have the choice on the size of the signature analyzer.

Tables 4, 5 and 6 summarize hardware overhead and test length required in the proposed design. They also compare them with other design techniques. These tables show that the proposed design requires minimum hardware overhead for large PLAs. From Table 5, it is also seen that if a Johnson counter with two level decoder circuitry (Liu & McCluskey 1987) is used as TPG2, the hardware overhead in the present design becomes very low. Its fault detection capability is comparable to Liu and McCluskey's (1987) design.

Data presented in Tables 4, 5 and 6 have been obtained based on computational results. Required additional space on chip for the self-test circuitry of BIST PLAs vary with the size of the actual PLA. Any figure on additional silicon space due to BIST circuitry is out of the scope of this paper as it presents only the computational results.

3. Response Evaluation Signature analyzer (SA) is a good response evaluator with a confidence level of $(1 - 2^{-k})$, where k is the length of the SA (Bardell, et. al. 1987). For a SA of length 8 ($= k$), this confidence level is about 0.9961. Counter based RES count the same value for a missing and an extra crosspoint device at a time in the same column, hence the error remains undetected. However, if such misplaced crosspoint device generates a different output sequence, it will be detected by both the parity check register RE and the signature analyzer SA. But parity check register cannot detect even parity faults. The above discussion proves that signature analyzer is the best solution as RE.

CONCLUSION

This paper proposed an optimized built-in self-test PLA design scheme. It applies universal test set. Its fault coverage is very high. It overcomes drawbacks introduced by parity checker and counter based response evaluators. It can be easily implemented following simple design procedures.

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