Jurnal Kejuruteraan 36(4) 2024: 1399–1407
https://doi.org/10.17576/jkukm-2024-36(4)-06

Dynamic Power Saving for CMOS Circuits

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Received 5 April 2023, Received in revised form 12 March 2024
Accepted 12 April 2024, Available online 30 July 2024

ABSTRACT

With more functionalities being integrated into a microchip today, higher processing power is drawn. As a result of this, clock and logic power consumption has turned out to be a critical issue to be coped with by chip designers. In this paper, we present various power-saving approaches employed in complementary metal oxide semiconductor (CMOS) circuit designs. The approaches involve restructuring the logic circuits, performing clock gating, and selecting the appropriate circuits for counters and frequency divisions. In order to show their efficacies in power optimization, the approaches were applied to a phase-locked loop (PLL), clock divider (CD), full adder (FA), counter, arithmetic logic unit (ALU), and microprocessor without interlocked pipelined stages (MIPS) circuits and validated using Intel Quartus Prime Lite and Mentor Graphics Modelsim. The following conclusions can be drawn from the results: Firstly, the efficacy of minimizing power dissipation using logic restructuring is found to be in direct proportion with the rate of the switching activity (SA); secondly, a maximum of 3.5% of thermal power dissipation can be saved using clock gating; thirdly, gray counters give the lowest power consumption; and, finally, the thermal power estimation for the phase-locked loop (PLL) is relatively higher than that for the clock divider (CD) when both of them are implemented for dividing frequencies.

Keywords: Power consumption; logic restructuring; clock gating; counter; frequency division

INTRODUCTION

The technological advancement of microchips has progressed in leaps and bounds. Within the span of half a century, the number of transistors that can be fabricated in a chip and the speed of which have increased close to 500 and 5000 times, respectively (Yeap et al. 2020; Yeap et al. 2019; Ho et al. 2016). The need to persistently improve the performance of a microchip is primarily driven by the insatiable demand to incorporate more functionalities into it. Take for instance, the microchip embedded in a mobile smartphone today. An advanced smartphone equipped with state-of-the-art technology may be accommodated with the fifth generation (5G) telecommunication, neural engine (NE), artificial intelligence (AI), augmented reality (AR), cloud computing, as well as, facial and speech recognitions features. In order to support these features, a microchip capable of sustaining higher processing power is therefore necessary. This, however, can only be attained at the expense of higher clock and logic power consumptions.

In general, the total power consumption P_{total} in a complementary metal oxide semiconductor (CMOS) circuit constitutes the dynamic power $P_{dynamic}$ (Agarwal and Nowka 2007) and the static power P_{static} (Butts and Sohi 2000), i.e. (Kim et al. 2003; Goel and McKee 2016; Zhu, Li, and Chen (2019):

$$P_{total} = P_{dynamic} + P_{static} \quad (1)$$

Dynamic power refers to the power consumed by the circuits when the transistors are operating in the active mode. CMOS circuits dissipate dynamic power whenever there are switching activities (i.e., the change from logic 1 to 0 and vice versa) or short-circuits. Hence, dynamic power consumption is ensued from the active operations

of the clock and logic circuits. Static power, on the other hand, is the power leakage when the transistors are inactive. To optimize power consumption in a CMOS circuit, it is important to minimize both static and dynamic power dissipations.

The power dissipations due to switching activities P_{switch}, short-circuits P_{short}, and current leakage P_{leak} are given in (2) to (4) below (Ng et al. 2022),

$$P_{switch} = C_{dyn} f_{clk} V_{DD}^{2}, \quad (2)$$

$$P_{short} = T_{sc} V_{DD} I_{peak}, \quad (3)$$

$$P_{leak} = V_{DD} I_{leak}, \quad (4)$$

where C_{dyn} is the dynamic effective capacitance, f_{clk} the clock frequency, V_{DD} the voltage supply, T_{sc} the time of logic transition, and I_{peak} is the peak current. While P_{short} and P_{leak} in (3) and (4) vary linearly with V_{DD}, it can be seen that P_{switch} in (2) varies quadratically. This is to say that, the contribution of the dynamic power to the overall power consumption is significantly higher than that of the static power, as long as the leakage current I_{leak} is contained within a reasonably low level. In a CMOS circuit, P_{short} only occupies a scanty fraction of the total power consumption (Gupta et al. 2004). Hence, P_{switch} has turned out to be the predominant factor for dynamic power dissipation (Magen et al. 2004; Kabbani, 2010) and developing ways to reduce switching activities have, therefore, become the key concern for minimizing P_{switch}. In this paper, we investigate and analyze various mechanisms which could be employed to minimize P_{switch}.

METHODOLOGY

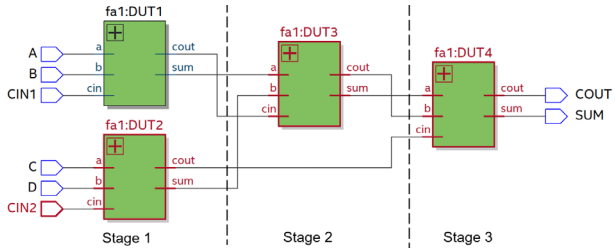
In general, power dissipations correspond directly with the frequency of switching activities. In order to optimize dynamic power consumption, it is therefore imperative to reduce the switching activities of circuits. Here, we investigate the efficacy of reducing the switching activities by restructuring the connections of the logic circuits, introducing clock gating to the circuits, and identifying the appropriate circuit for counters and frequency divisions (Microsemi, 2012). These approaches were applied to phase-locked loop (PLL), clock divider (CD), full adder (FA), counter, arithmetic logic unit (ALU), and microprocessor without interlocked pipelined stages (MIPS) circuits and validated using Intel Quartus Prime Lite and Mentor Graphics Modelsim. It is worthwhile noting here that the approaches were applied according to the functions of the circuits.

RESULTS AND DISCUSSION

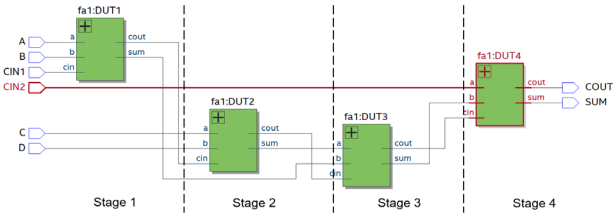
LOGIC RESTRUCTURING

Logic restructuring is the process of rearranging the connection of a circuit with the aim of achieving certain desired purposes and without altering the original functionality of the circuit. The desired purposes may vary according to the design need of the chip. Some examples of which include to meet the timing requirement, to avoid routing congestion, to enhance the speed of the chip, to optimize the design area, etc. For our case, the purpose of doing so is, of course, to minimize the dynamic power consumption.

In order to validate its effectiveness in power saving, logic restructuring is applied to a 2-bit full-adder (FA). As can be seen in Figure 1, a 3-stage 2-bit FA is reconstructed into four stages. Four 1-bit FA (indicated by *fa*1 in the figure) were used as the building blocks for the 2-bit FAs. It can be observed from both figures that, the 3-stage and 4-stage structures comprise the same number of building blocks. The order of these blocks is, however, rearranged. The *CIN*2 pin is assigned with high switching activities; while, the rest of the input pins (i.e., *A*, *B*, *C*, *D*, and *CIN*1) are connected to a common signal with relatively lower switching activities.

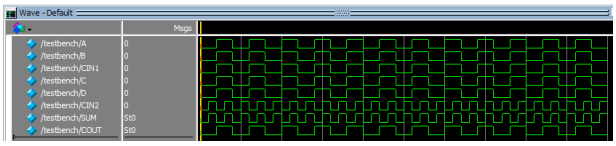


(a)

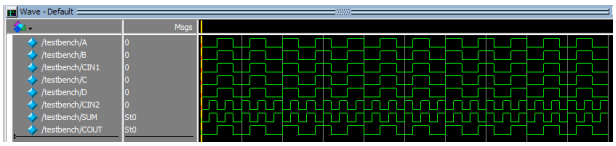


(b)

FIGURE 1. The schematics of a (a) 3-stage and (b) 4-stage 2-bit full adder

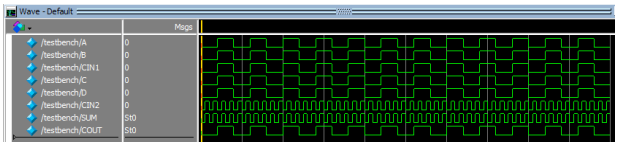


(a)

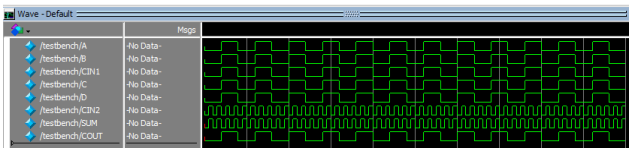


(b)

FIGURE 2. Timing diagrams of the (a) 3-stage and (b) 4-stage 2-bit full adders when *CIN*2 is supplied with a 50 MHz signal

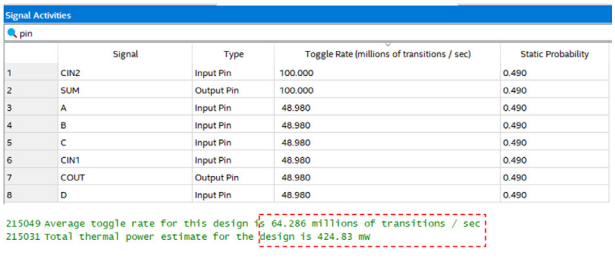


(a)

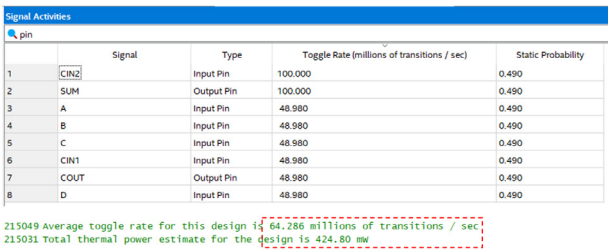


(b)

FIGURE 3. Timing diagrams of the (a) 3-stage and (b) 4-stage 2-bit full adders when *CIN*2 is supplied with a 100 MHz signal

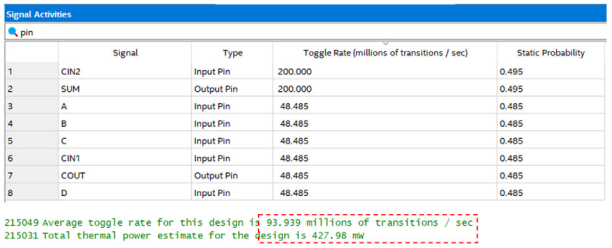


(a)

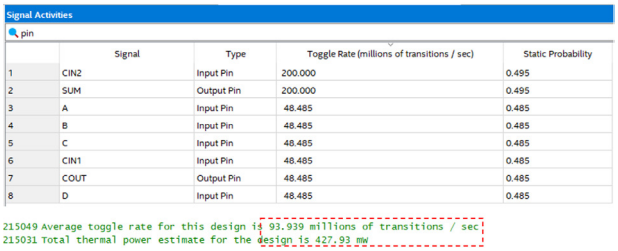


(b)

FIGURE 4. Signal activities of the (a) 3-stage and (b) 4-stage 2-bit full adder when *CIN*2 is fed with a 50 MHz signal



(a)



(b)

FIGURE 5. Signal activities of the (a) 3-stage and (b) 4-stage 2-bit full adder when *CIN*2 is fed with a 100 MHz signal

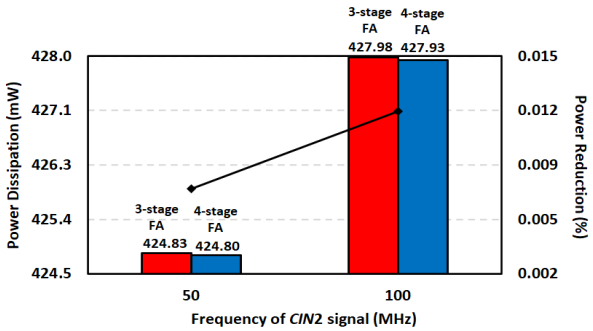


FIGURE 6. Thermal power dissipations of the 3- and 4-stage 2-bit full adder

The main reason for reconstructing the FA from three to four stages is to shift the pin with high switching activity (SA) to the last stage. In the 3-stage FA, a high SA signal is applied at the first stage via *CIN*2. The signal tends to propagate downstream, toggling the other two blocks at the subsequent stages. Since the switching rate is high, power consumption at these three blocks turns out to be comparatively higher than that connected only to the *A*, *B*, and *CIN*1 pins. To reduce the switching activities at the intermediate blocks, the circuit is modified with *CIN*2 shifted to the last stage. The high SA signal is therefore modelled as the late-arriving signal. Doing so, only the circuit block at the last stage would now be toggling at a fast rate, while the other blocks are spared.

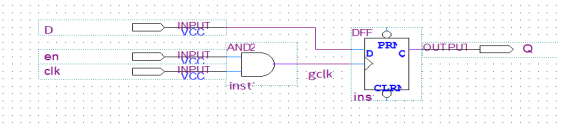
To determine the relationship between the SA and the power consumption, two test cases were simulated. In the first case, *CIN*2 is supplied with a 50 MHz signal, and in

the second, the signal is increased to 100 MHz. The input frequency for *A*, *B*, *C*, *D*, and *CIN*1 are set at a constant rate of 25 MHz. Figures 2 and 3 depict the timing diagrams obtained from the functional verification. Clearly, the 3- and 4-stage FAs are in good agreement with each other and that they produce the intended result of an adder. The thermal power estimations for both structures are shown in Figures 4 and 5. When *CIN*2 is assigned with a 50 MHz signal, Figure 4 indicates that the power consumption of the adder drops from 424.83 mW to 424.80 mW after the restructuring process. Although a 0.03 mW of power reduction may seem trivial, it is to be noted that, this diminutive amount only applies to a single 2-bit FA circuit. In reality, an advanced high-speed microprocessor may easily comprise hundreds of such adders. With each of the adders restructured, the cumulative amount of power saved in a microchip will certainly turn out to be hefty. When the signal at *CIN*2 is increased to 100 MHz, it can be seen from Figure 5 that the power consumptions before and after restructuring are, respectively, 427.98 mW and 427.93 mW. A 0.05 mW power is saved in this case. A summary of power saving at input frequency f = 50 MHz and 100 MHz is depicted in Figure 6. The results suggest that the efficacy of minimizing power dissipation using logic restructuring is in direct proportion with the rate of the SA.

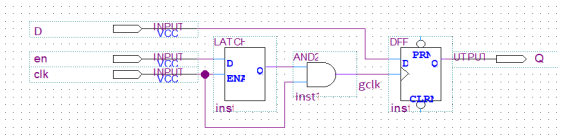
CLOCK GATING

Chip designers usually apply clock gating to turn off design blocks which are dormant. Figure 7(a) shows a simple clock gating circuit built using an AND gate. As can be seen in the figure, an additional "clock enabled" *en* pin is introduced to the input of the AND gate to activate the clock signal fed to the flip-flop. When the flip-flop is inactive, the clock signal can be switched off by assigning a logic 0 to the *en* pin. Owing to the signal delay at the *en* pin, however, glitches may sometimes occur at the output of the AND gate. To overcome this drawback, a latch is added between the *en* pin and the AND gate, as depicted in Figure 7(b). Here, the latch-based clock gating is applied to a 4-bit counter, an 8-bit arithmetic logic unit (ALU), and a 16-bit microprocessor without interlocked pipelined stages (MIPS).

Figures 8 to 10 show the schematics of the 4-bit counter, 8-bit ALU, and 16-bit MIPS, with and without the clock gating circuit installed into them. The timing diagrams in Figures 11 to 13 corroborate the functionalities of the circuits. Figure 14 summarizes the thermal power consumptions extracted from the signal activities in Figures 15 to 17. With the incorporation of the clock gating circuit, it can be seen that the counter, ALU, and MIPS have saved about 0.12%, 0.16%, and 3.5% of thermal power dissipations, respectively. Indeed, power reduction is particularly evident when the technique is applied to the MIPS.

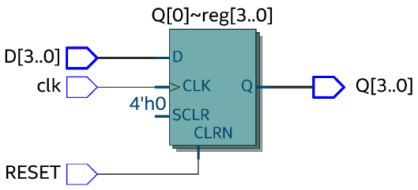


(a)

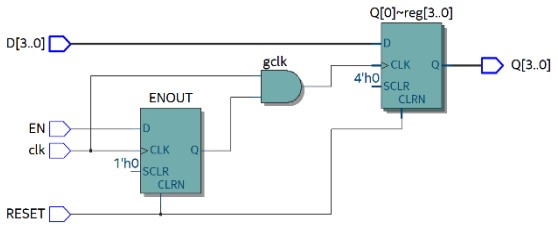


(b)

FIGURE 7. A (a) basic clock gating circuit using an AND gate and a (b) latch-based clock gating circuit using a D-latch and an AND gate

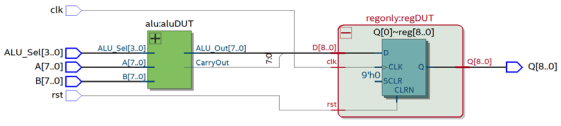


(a)

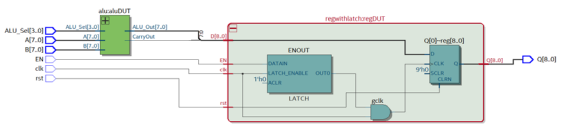


(b)

FIGURE 8. A 4-bit counter (a) without and (b) with clock gating

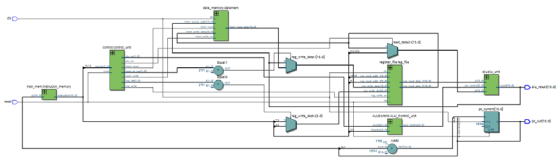


(a)

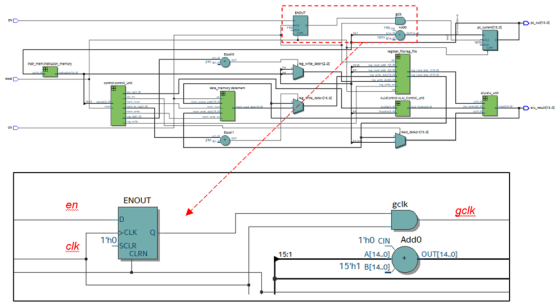


(b)

FIGURE 9. An 8-bit ALU (a) without and (b) with clock gating

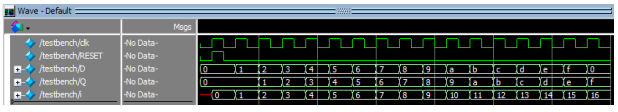


(a)

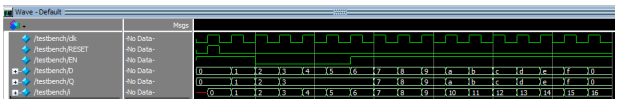


(b)

FIGURE 10. A 16-bit MIPS (a) without and (b) with clock gating. A closer view of the clock gating circuit is shown in the inset in (b)

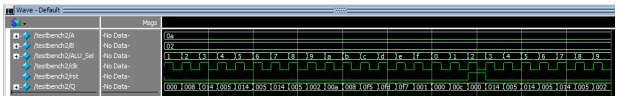


(a)

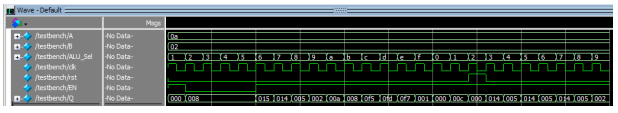


(b)

FIGURE 11. Timing diagrams of the 4-bit counter (a) without and (b) with clock gating

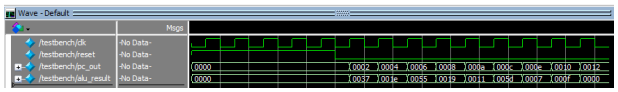


(a)

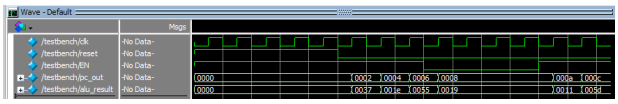


(b)

FIGURE 12. Timing diagrams of the 8-bit ALU (a) without and (b) with clock gating



(a)



(b)

FIGURE 13. Timing diagrams of the 16-bit MIPS (a) without and (b) with clock gating

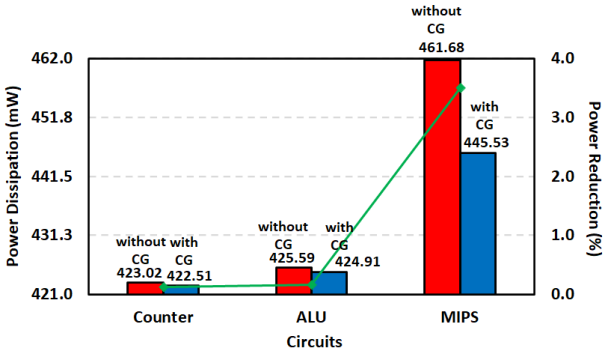


FIGURE 14. Thermal power dissipations of the circuits without and with clock gating (CG)

Signal Activities

pin

	Signal	Type	Toggle Rate (millions of transitions / sec)	Static Probability
1	clk	Input Pin	100.000	0.500
2	D[0]	Input Pin	47.059	0.471
3	Q[0]	Output Pin	44.118	0.441
4	D[1]	Input Pin	23.529	0.471
5	Q[1]	Output Pin	20.588	0.441
6	D[2]	Input Pin	11.765	0.471
7	Q[2]	Output Pin	8.824	0.441
8	D[3]	Input Pin	5.882	0.471
9	RESET	Input Pin	5.882	0.029
10	Q[3]	Output Pin	2.941	0.441

215049 Average toggle rate for this design is 29.804 millions of transitions / sec
215031 Total thermal power estimate for the design is 423.02 mW

(a)

Signal Activities

pin

	Signal	Type	Toggle Rate (millions of transitions / sec)	Static Probability
1	clk	Input Pin	100.000	0.500
2	D[0]	Input Pin	47.059	0.471
3	Q[0]	Output Pin	35.294	0.588
4	D[1]	Input Pin	23.529	0.471
5	Q[1]	Output Pin	17.647	0.588
6	D[2]	Input Pin	11.765	0.471
7	Q[2]	Output Pin	11.765	0.294
8	D[3]	Input Pin	5.882	0.471
9	EN	Input Pin	5.882	0.765
10	Q[3]	Output Pin	5.882	0.471
11	RESET	Input Pin	5.882	0.029

215049 Average toggle rate for this design is 23.693 millions of transitions / sec
215031 Total thermal power estimate for the design is 422.51 mW

(b)

FIGURE 15. Signal activities of the 4-bit counter (a) without and (b) with clock gating

Signal Activities

pin

	Signal	Type	Toggle Rate (millions of transitions / sec)	Static Probability
1	clk	Input Pin	100.000	0.510
2	ALU_Sel[0]	Input Pin	48.980	0.510
3	Q[0]	Output Pin	28.571	0.408
4	Q[4]	Output Pin	28.571	0.367
5	ALU_Sel[1]	Input Pin	24.490	0.490
6	Q[2]	Output Pin	16.327	0.653
7	Q[3]	Output Pin	16.327	0.204
8	ALU_Sel[2]	Input Pin	12.245	0.490
9	Q[1]	Output Pin	10.204	0.143
10	ALU_Sel[3]	Input Pin	6.122	0.388

215049 Average toggle rate for this design is 4.540 millions of transitions / sec
215031 Total thermal power estimate for the design is 425.59 mw

(a)

Signal Activities

pin

	Signal	Type	Toggle Rate (millions of transitions / sec)	Static Probability
1	clk	Input Pin	100.000	0.510
2	ALU_Sel[0]	Input Pin	48.980	0.510
3	ALU_Sel[1]	Input Pin	24.490	0.490
4	Q[0]	Output Pin	24.490	0.367
5	Q[4]	Output Pin	20.408	0.327
6	Q[2]	Output Pin	16.327	0.531
7	Q[3]	Output Pin	16.327	0.327
8	ALU_Sel[2]	Input Pin	12.245	0.490
9	Q[1]	Output Pin	10.204	0.143
10	ALU_Sel[3]	Input Pin	6.122	0.388

215049 Average toggle rate for this design is 4.371 millions of transitions / sec
215031 Total thermal power estimate for the design is 424.91 mw

(b)

FIGURE 16. Signal activities of the 8-bit ALU (a) without and (b) with clock gating

Signal Activities

pin

	Signal	Type	Toggle Rate (millions of transitions / sec)	Static Probability
1	clk	Input Pin	100.000	0.500
2	alu_result[2]	Output Pin	57.143	0.429
3	alu_result[0]	Output Pin	42.857	0.500
4	alu_result[3]	Output Pin	42.857	0.286
5	alu_result[1]	Output Pin	35.714	0.286
6	alu_result[4]	Output Pin	35.714	0.429
7	alu_result[5]	Output Pin	35.714	0.071
8	alu_result[6]	Output Pin	35.714	0.143
9	pc_out[1]	Output Pin	32.143	0.321
10	alu_result[7]	Output Pin	28.571	0.000

215049 Average toggle rate for this design is 3.071 millions of transitions / sec
215031 Total thermal power estimate for the design is 461.68 mw

(a)

Signal Activities

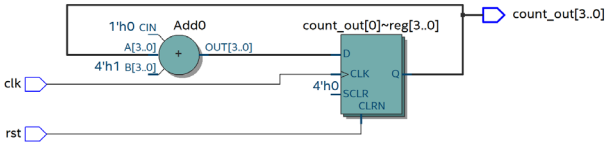
pin

	Signal	Type	Toggle Rate (millions of transitions / sec)	Static Probability
1	clk	Input Pin	100.000	0.500
2	alu_result[2]	Output Pin	32.143	0.250
3	alu_result[5]	Output Pin	28.571	0.071
4	alu_result[0]	Output Pin	25.000	0.536
5	alu_result[3]	Output Pin	25.000	0.393
6	alu_result[4]	Output Pin	25.000	0.607
7	alu_result[6]	Output Pin	25.000	0.107
8	alu_result[1]	Output Pin	21.429	0.143
9	alu_result[7]	Output Pin	21.429	0.000
10	alu_result[8]	Output Pin	21.429	0.000

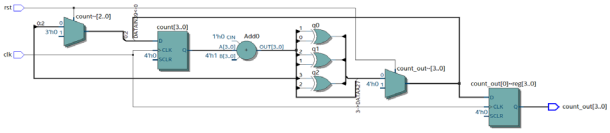
215049 Average toggle rate for this design is 1.161 millions of transitions / sec
215031 Total thermal power estimate for the design is 445.53 mw

(b)

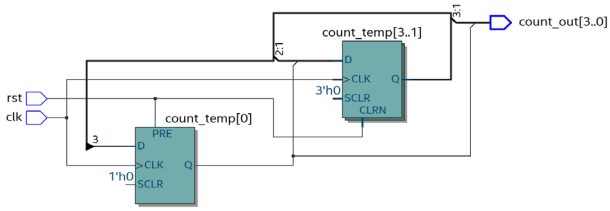
FIGURE 17. Signal activities of the 16-bit MIPS (a) without and (b) with clock gating



(a)



(b)

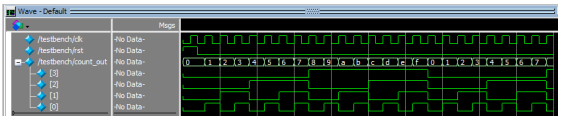


(c)

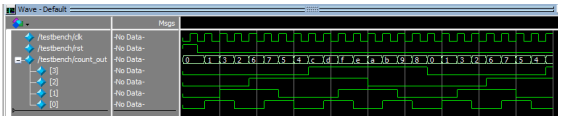
FIGURE 18. The schematics of a (a) binary counter, a (b) Gray counter, and a (c) ring counter

COUNTERS

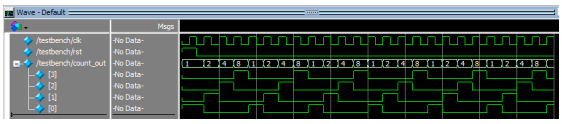
In digital circuits, counters are used to keep track of the rate of occurrence of an activity or instance. Here, the power consumptions of the three most common counters, namely, the binary, Gray, and ring counters are analyzed. Figure 18 shows the schematics for the different types of counters. As can be seen from the functional verifications in Figure 19, the three types of counter circuits in Figure 18 are working in order. The SA of the counters are depicted in Figure 20 and summarized in Figure 21. It is apparent that the Gray counter gives the most promising outcome – the power consumption is, respectively, 1.22 mW and 1.39 mW lower than the binary and ring counters. This result is somewhat to be expected since the timing diagrams in Figure 19 clearly show that the Gray counter only changes a single bit at each transition; whereas, the other two of its counterparts may change more than a bit.



(a)

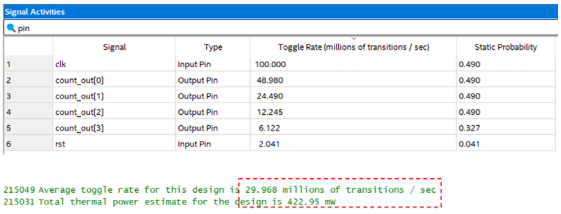


(b)

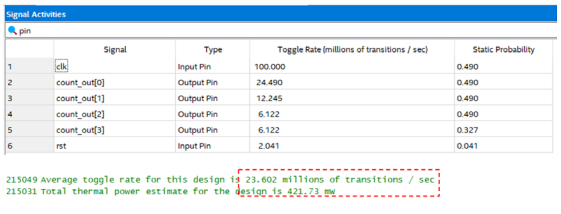


(c)

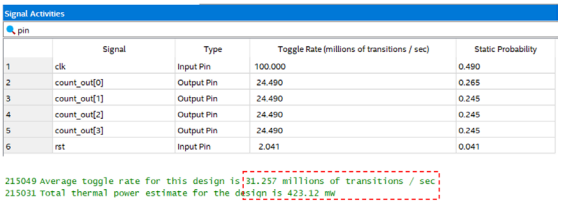
FIGURE 19. Timing diagrams of the (a) binary, (b) Gray, and (c) ring counters



(a)



(b)



(c)

FIGURE 20. Signal activities of the (a) binary, (b) Gray, and (c) ring counters

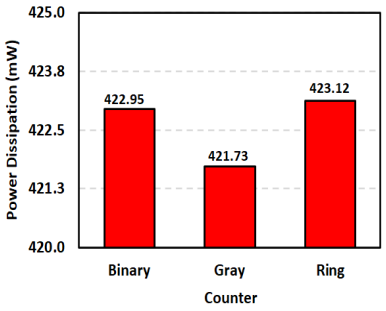


FIGURE 21. Thermal power dissipations of different types of counters

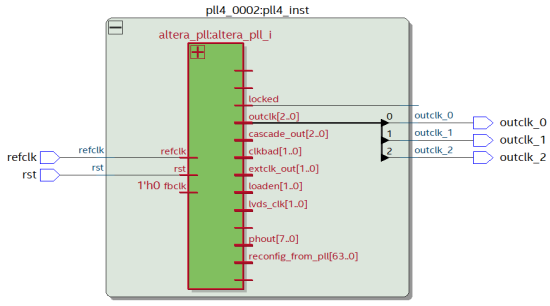


FIGURE 22. The phase-locked loop provided by Intel Quartus Prime IP block

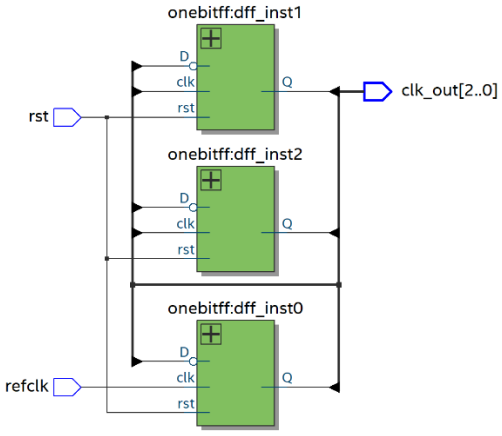
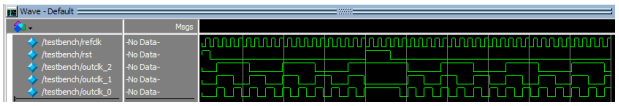
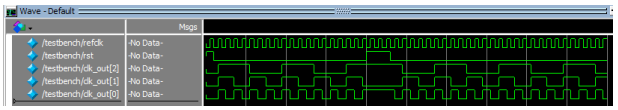


FIGURE 23. The schematic of a clock divider

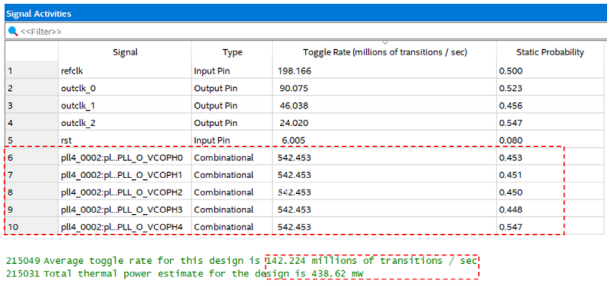


(a)

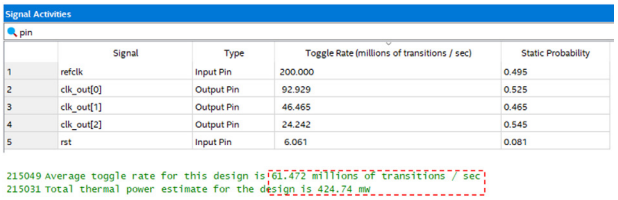


(b)

FIGURE 24. Timing diagrams of the (a) phase-locked loop and (b) clock divider



(a)



(b)

FIGURE 25. Signal activities of the (a) phase-locked loop and (b) clock divider

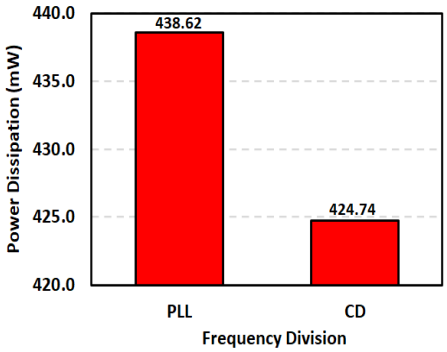


FIGURE 26. Thermal power dissipations of a phase-locked loop (PLL) and a clock divider (CD) when performing frequency division

FREQUENCY DIVISION

A phase-locked loop (PLL) is a closed-loop control system which synchronizes the phase and frequency of the output signal with those of the input (Ahmadzadeh, Mortazavi, and Saniei, 2018). Since PLLs are readily embedded in microcontrollers and field programmable gate arrays (FPGAs), they are commonly used to perform frequency divisions. In reality, a PLL serves various other functions as well. Besides frequency division, it is also used for frequency multiplication, phase shifting, and delay operations (Microsemi, 2012). Because of this reason, a PLL may consume redundant power unnecessarily, if it is used only for specific functions. Here, we compare the power consumptions of a PLL and a clock divider (CD) implemented solely for dividing frequencies (Wahab and Kamal, 2018). Figures 22 and 23 show the schematics of the PLL and CD. It is to be noted that, the PLL used here is adopted from the intellectual property (IP) block provided by Intel Quartus Prime. Both the PLL and CD are designed to generate three output frequencies, namely, 50 MHz, 25 MHz, and 12.5 MHz, based on the 100 MHz reference input frequency. The functionalities of the two devices are verified in Figure 24. As can be seen in Figures 25 and 26, the thermal power estimation for the PLL is relatively higher than that for the CD. This is attributed to the high SA found in the internal combinational logics of the PLL (i.e., row 6 to 10 of Figure 25(a)). It can also be observed from Figure 26 that, 13.88 mW (approximately 3.16%) of power is saved when the PLL is substituted with a CD.

CONCLUSION

We have analyzed various approaches used to minimize clock and logic power consumptions. In the first approach, we re-organized the logic blocks, so that the input with high switching activities was shifted to the last stage. Doing so, the power drawn by the logic blocks at the earlier stages could be reduced. In the second approach, an additional switch (i.e., an AND gate) was introduced into the existing circuits. The switch was used to disable the circuit block when it was inactive, thereby saving unnecessary drainage power. We also compared the efficiency of three different common types of counters in our third approach. Since Gray counter only changes a single bit at each transition, it was found to consume the least power. In our last approach, a clock divider (CD) was suggested to substitute a phase-locked loop (PLL) when performing frequency division. Since a PLL is capable of serving multiple functions, the combinational logics within is inherently more complicated. A PLL is therefore more power hungry when it is used for limited purposes.

ACKNOWLEDGMENT

The authors would like to thank the department of civil engineering, Mehran University of Engineering and Technology Jamshoro for their support.

DECLARATION OF COMPETING INTEREST

None

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